

RESEARCH ARTICLE

Study of Electrical Properties of Photodetector

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ABSTRACT

In this paper porous silicon sample that can be used as a photodetector was prepared at fixed etching time of 15min and different etching current density (15, 17, 19 and 21) mA/cm². Electrical properties of Al / PSi / p-Si /Al photodetector were studied. We found that the I-V characteristics dependence of the etching current density relates to the PSi pores development, where the pore diameter in PSi structure might get enlarged due to the enhancement of the etching current density. The ideality factor ranges around (6.8-4.2) while the barrier height decreased with the increasing etching current density and the etching time as the interface layer between PSi/c-Si has large amount of pinning. Then the C-V characteristics of the sandwich structure are described. When the etching current densities are increased, it reduces the capacitance of the PSi layer. It thus increases the thickness of the depletion region which in turn results in development of built-in potential.

Keywords: Porous silicon, Etching current density, Electrical properties, Photodetector, I-V/C-V characteristics.

1. INTRODUCTION

The demand of effective compact equipment is growing widely for vast applications comprising numerous sectors. Among the candidate materials, Porous silicon (PSi) has drawn the attention of many researchers, besides its possibility to integrate PSi directly with the standard silicon technologies, and its present applications span from biomedicine to bio-sensing and from photonics to photovoltaic devices [1]. Four major causes that have led to the continued widespread attention to PSi are the following [2]:

1. Its efficient visible luminescence gives rise to the opportunity of all-Si-based optoelectronic components.
2. Its compatibility with current silicon microelectronic processing makes integrated silicon based optoelectronic devices a reality.
3. Its production is less costly and simple.

4. Its larger surface-to-volume ratio makes the porous silicon matrix an excellent host of biological and chemical species.

2. ELECTRICAL PROPERTIES

Optoelectronic applications including light-emitting devices, photo detectors and solar cells using PSi active layer require proper understanding of electronic transport behaviour of PSi layers in device structure, especially the properties of the junction. The transport of carriers within the PSi layer thickness and across the PSi/c-Si heterojunction governs the device characteristics [3].

Electrical resistivity in PSi increases with increasing porosity as PSi gets depleted by free carriers. Depletion occurs due to energy gap widening from quantum confinement, that decreases the free carrier's thermal generation, or due to free carriers trapping occurring during porous Si formation with respect to the development of surface states. There is also loss

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of charge carriers due to their compensation by surface states [4]. Reverse current exhibits soft breakdown voltage. This performance is an indication of the carrier transport through hetero structure. It elaborated the most common attributes in order to describe the rectifying characteristics of PSi diodes:

- Supply of minority carriers from the Si substrate or barrier at the PSi/Si junction.
- Schottky barrier at the contact Al/PSi junction.
- P-N junction within PSi layer for PSi made from a c-Si p-n junction [5].

2.1. Dark Current-Voltage (I-V) characteristics

I-V characteristics curves can be fitted well by equation (2.1) of thermionic emission theory.

$$I(V) = I_s \left[\exp\left(\frac{qV}{ZK_B T} - 1\right) \right] \quad (2.1)$$

where V is the voltage across the device, Z is called the slope parameter or ideality factor (which is equal to 1 for the ordinary Schottky devices-it is a parameter which can show the ideality of fabricated devices), q is charge of electron, K_B is the Boltzmann constant at room temperature T and I_s is the saturation current which is governed by thermionic emission equation (2.2) [6, 7].

$$I_s = A' A^* T^2 \exp\left(\frac{-q\phi_B}{K_B T}\right) \quad (2.2)$$

where A* refers to the effective Richardson's constant, which equals 32(A/K².cm²) for p-type silicon, A' denotes the surface area of PSi and φ_B (eV) is the barrier height that is calculated using equation (2.3).

$$\phi_B = \frac{K_B T}{q} \ln \frac{A^* A' T^2}{I_s} \quad (2.3)$$

Z of Al /PSi/c-Si/Al surface type Schottky diode can be computed by means of current-voltage characteristics according to equation (2.4).

$$Z = \frac{q}{K_B T} \left[\frac{dV}{d \ln I} \right] \quad (2.4)$$

2.2. Dark Capacitance-Voltage (C-V) characteristics

Capacitance measurements offer a valuable tool for investigating the electrical properties of PSi layer and devices containing PSi layer [8]. The capacitance of PSi layer depends on its morphological properties since it decreases with the increasing thickness of the layer [9].

3. EXPERIMENTAL WORK

The practical part is described as stated below.

3.1. Substrate preparation

Initially the impurities and remains from the surface of p-type Si samples are removed using alcohol in an ultrasonic bath. These substrates were cut into (1cm×1cm) compatible size with the dimension of substrate holder by using a steel cutter tool and etched with HF (40%) for 5min to remove the native oxide. Thin homogenous PSi layer of various thicknesses is formed on the frontal surface of the material using Electro-Chemical Etching method (ECE).

3.2. Preparation of porous silicon layer

The next section describes the preparation of porous silicon:

3.2.1. Electrodes deposition

The bottom electrode is covered with a thick Al layer in advance to the anodization procedure. In order to measure the electrical properties, ohmic contacts are needed. It is obtained under vacuum of aluminum wire of high purity (99.99%). The evaporation process is started at a pressure of 10⁻⁵ Torr.

3.2.2. Electrochemical etching process

Crystalline wafers of p-type Si with resistivity (1-10)Ωcm, 565μm thickness and 100⁰ orientation are employed as starting substrate which is then split into square with dimension of 1cm×1cm. It is followed by electrochemical etching in a blend of 1:1 hydrogen fluoride (40%) - ethanol (99.98%) at normal temperature using a gold electrode. The schematic setup of electrochemical etching is depicted in figure 1. Sample prepared at different etching current density (15, 17, 19, 21)mA/cm², where the

etched area in the sample is 1cm^2 as shown in figure 2.

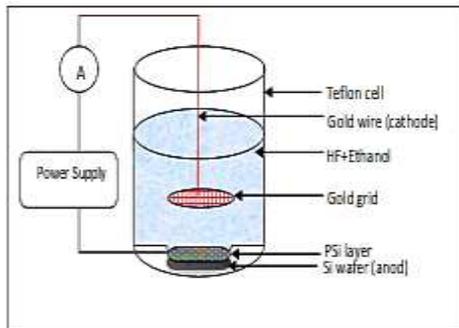


Figure 1. Electrochemical etching set –up



Figure 2. Prepared PSi samples

4. DEVICES MEASUREMENT

The electrical properties of the nanostructure of photo detector were studied. All measurements were carried out in both dark room and day illumination. The electrical measurement involved current-voltage and capacitance- voltage measurements.

4.1. Current-voltage measurements

The requirements of current–voltage measurement are,

- UNI-T-UT33C digital electrometer
- Tektronics CDM 250 multimeter
- Dual Farnel LT30/2
- 0 to 10V power supply

Positive voltage was supplied to aluminum metal contact with the nanostructure layer in relation with the aluminum electrode over the crystalline Si substrate, and the forward current is noted.

4.2. Capacitance –voltage measurements

Capacitance measurements as functions of reverse voltage (C-V) for PANI- incorporated PSi/p-Si/Al structure are carried out using LCZ meter at a frequency of 100 kHz. The built in potential (V_{bi}) as well as the barrier height for both the devices are calculated. The relation of

finding the barrier height is given in equation (2.3).

5. RESULTS AND DISCUSSIONS

In this part we show the results and the connected discussions for Al / PSi / p-Si /Al photodetector.

5.1. Electrical properties of Al / PSi / p-Si /Al photodetector

The interest to study the electrical and photoelectrical properties of PSi layer appears first of all from prospects of several technological developments of applications such as detectors, solar cells, sensors, etc. [10]. I-V and photovoltaic characteristics and such related electrical parameters such as ideality factor, rectification ratio and the charge carrier transport mechanisms in Al/PSi/c-Si/Al sandwich structure depend on the structural attributes of PSi layer. We have studied the electrical and photoelectrical characteristics of Al/PSi/p-Si/Al structure apart from investigating the effect of structural parameters of the PSi layer on these properties. By considering all these factors, the PSi layers are prepared at different etching current density (15, 17, 19, 21) mA/cm^2 with constant etching time of 15min for p-type silicon.

5.2. C-V characteristics of Al/p-PSi/p-Si/Al in dark

Figure A1 illustrates the Schottky or heterojunction behaviour. It relates the etching current density-voltage features of Al/PSi/p-Si/Al structure formed at 15min. It is of dissimilar etching current densities (15, 17, 19 and 21) mA/cm^2 in which the current-voltage graphs are attained by varying the applied bias (ranging from -10 V to +10 V). Then the resultant etching current density is measured.

Figure A1 shows the forward and reverse current at room temperature under dark conditions as a function of applied bias voltage. The maximum value of forward and reverse current for bias voltage of 10V is 2.7mA and $3.2\mu\text{A}$ respectively, for sample prepared with 15 mA/cm^2 etching current density, while the minimum value of forward and reverse current is 1.24mA and $1.15\mu\text{A}$ respectively for sample prepared with 21 mA/cm^2 etching current density.

The dependence of I-V characteristics on the etching current density relates to the Psi pore development. Here the pore diameter of the PSi structure might get enhanced when the etching current density is increased, which in turn increases PSi resistivity with respect to the carrier trapping at pores wall. This further minimizes the current for all forward and reverse biases because of the reduced mobility in the increasing PSi layer, and this agrees [11, 12].

On the other hand, the sandwich structure shows a rectifying behaviour under the existence of PSi/p-Si heterojunction as illustrated in figure A1. The forward current of all our photodetectors is less than 3 V. It is said to be recombination current occurring only at low voltage, which is caused during electrons excitation from valence band in order to get the balance back. The other area of higher voltage indicates the diffusion or bending portion that depends on serried resistance. Here the bias voltage delivers electrons with sufficient energy to enter beyond the barrier within the dual junction sides [13].

Table 1 shows the ideality factor (Z) and the barrier height (eV) at different etching density.

Table 1.The characteristics of fabricated photodetectors

Etching time (min)	Etching current density (mA/cm ²)	Ideality factor(Z)	Barrier height (Φ _B)(eV)
15	15	4.6	0.388288
	17	3.9	0.362419
	19	2.5	0.354293
	21	2.3	0.332629

The values of the ideality factor are found to be around 4.6 to 2.3 at 15min etching time and different values of etching current density, (15, 17, 19, 21) mA/cm². If the structure includes interface states, ideality factor becomes high, that accounts to the totality of Z of the individual rectifying junctions (i.e., the actual PSi/c-Si heterojunction and Schottky diodes at the Al/PSi or the two metal-semiconductor junctions (Al/PSi, p-Si/Al) of a diode preferably possess Ohmic features) thus resulting in the ideal factor to be higher than unity. Interfacial oxide layer may also be the possible cause for a

higher ideality factor, where this result is similar to [14], while the barrier height decreased with the increasing etching current density. This etching current is enhanced in accordance to the interface layer between PSi/c-Si which has large amount of pinning, thus acting as a defect in the interface and causes to rise the saturation etching current density, thereby reducing the barrier height of PSi/c-Si, and this agrees with [15, 16].

5.3. Illuminated I-V characteristics (Photocurrent)

The photocurrent of PSi-based devices depends on the morphological and structural characteristics of porous silicon layer, especially in case of layer thickness and porosity.

Figure 3 illustrates the I-V characteristics of Al/PSi/p-Si/Al sandwich model of samples made at diverse etching current density (15, 17, 19, 21)mA/cm² and power intensity (540, 1230 and 1800)μW/cm² with constant etching time in dark conditions at room temperature.

Figures A2(a) and A2(b) show that when the etching current density increases, photocurrent decreases due to the increasing porosity and thickness. On the other hand, increasing the PSi porosity means a change in junction depth and diffusion length. Due to the illumination of structures, the electron-hole pairs produced in the depletion layer of PSi/c-Si heterojunction lessen the barrier for the electrons, where these results are in agreement with [17]. But the relationship of the I-V graphs denotes the photo-generated carriers where the related light absorption occurs at the depletion area.

From figures A2(a) and A2(b), we observed that when the photocurrent of PSi increases, the power intensity also increases. At 10V biasing and 1800μW/cm², the photocurrent of PSi formed at etching time 15min is greater than the PSi obtained at 21min which is due to the reduction of the permeability. When anodization time is increased, the current gets reduced with respect to its reduction in conductivity and enhancement in the width and pore diameter of PSi layer. Hence it shows that the resistivity is higher and these results were in good agreement with [18].

Figure 3 shows the variation of photocurrent with incident power density (540, 1230 and 1800) $\mu\text{W}/\text{cm}^2$ at 10V bias for the Al/PSi/p-Si/Al sample prepared at 19 mA/cm² etching current density and 15min etching time. When the sample is illuminated with the light of varying intensity, resistance gets reduced with the increasing photon energy of the illuminating light for all samples, possibly owing to the addition of electron hole-pairs. The photocurrent of PSi-based devices depends on the light power density. It increases with the incident power density, indicating that the Al/PSi/p-Si/Al junction can be used as a photo detector.

Increase in the light intensity increases the photocurrent also, and this relationship is called density characteristics of the photodetector (dynamic range). No significant saturation in photocurrent is observed at high level intensity of light. The photocurrent as well as increase in the depletion width leads to increase in the absorption through it and the creation of electron-hole pairs.

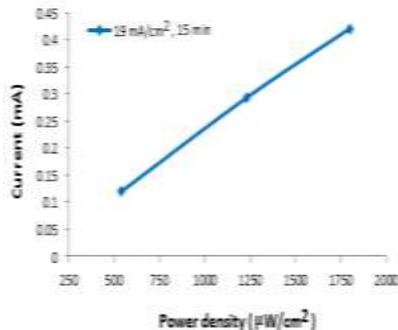


Figure 3. Linearity characteristic of Al/PSi/c-Si/Al heterojunction devices at bias

5.4. Capacitance –voltage measurements of Al/PSi/p-Si/Al

C-V characteristic is one of the most important parameters of Al/PSi/p-Si/Al heterojunction photodetector, since it controls various factors including built-in potential, depletion width layer and junction type.

Figure 4 illustrates the capacitance-voltage characteristics of the sandwich structure with different etching current density (15, 17, 19, 21) mA/cm² with constant etching time at 15min. It shows that the enhancement of the etching current density leads to the reduction of the capacitance of the PSi layer, which in turn

results in rise of the thickness of the depletion area thus raising the built-in potential [17]. It is clear in figures A3(a) and A3(b).

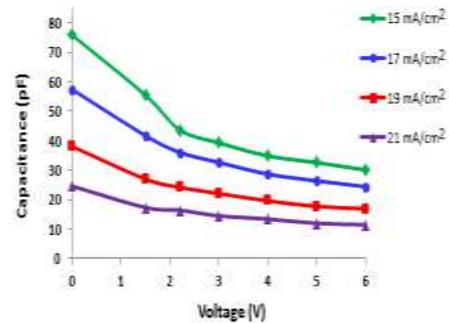


Figure 4. C-V characteristics of Al/PSi/p-Si/Al heterojunction at different etching current densities and 15min etching time

Figures A3(a) and A3(b) shows the relationship within the inverse capacitance squared and the reverse bias of the Al/PSi/p-Si/Al heterojunction in dark conditions at room temperature at the increment voltage of frequency 1000kHz for samples prepared at diverse current density and 15min etching time.

Due to the increasing depletion width region, the value of V_{bi} increases from 1.2V to 1.7V when etching current density increases. This linear relationship of C^{-2} with bias voltage shows that the junction is of rapid type which represents Schottky like barrier between Al layer and porous silicon. Calculation of built in potential (V_{bi}) is done by extrapolating ($1/C^2-V$), plot to ($1/C^2=0$). V_{bi} was calculated for Al/PSi/p-Si/Al heterojunction at various etching current density and 15min etching time.

6. CONCLUSIONS

1. The electrical properties imply that the prepared device has good linearity and is of abrupt type.
2. Electronic properties show that the formation of a heterojunction with such a forbidden gap of the two materials completely overlaps and is called staggered case.

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APPENDIX

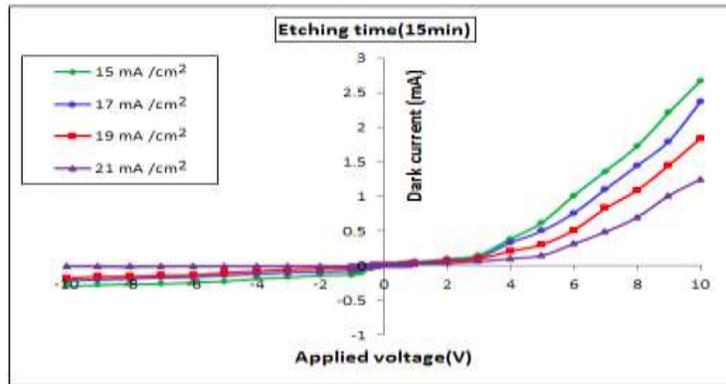


Figure A1. Dark I-V characteristic under forward and reverse bias of the Al/PSi/c-Si/Al

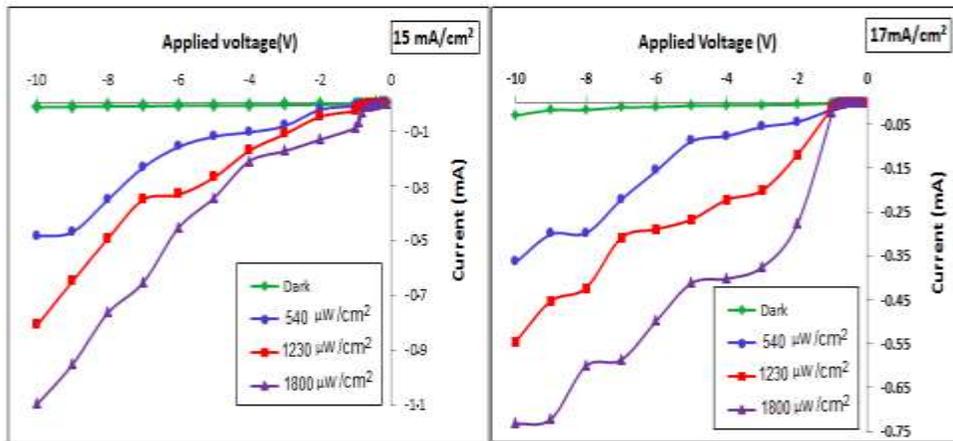


Figure A2(a). Dark and illuminated I-V characteristic of Al/PSi/c-Si/Al photodetector

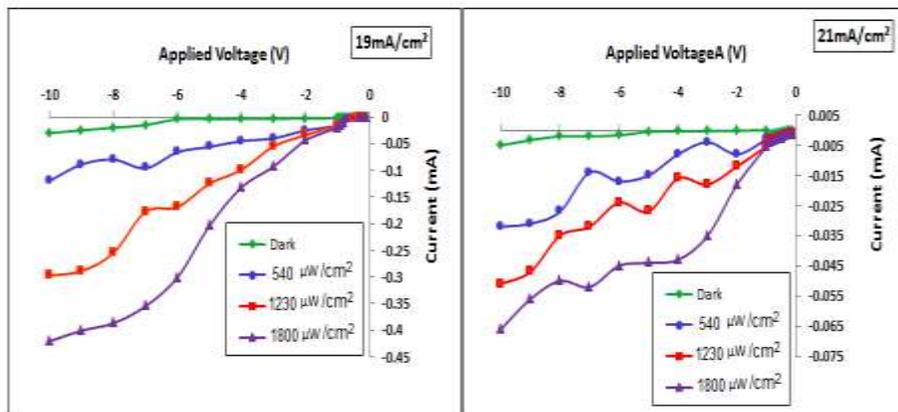


Figure A2(b). Dark and illuminated (I-V) characteristic of Al/PSi/c-Si/Al photodetector

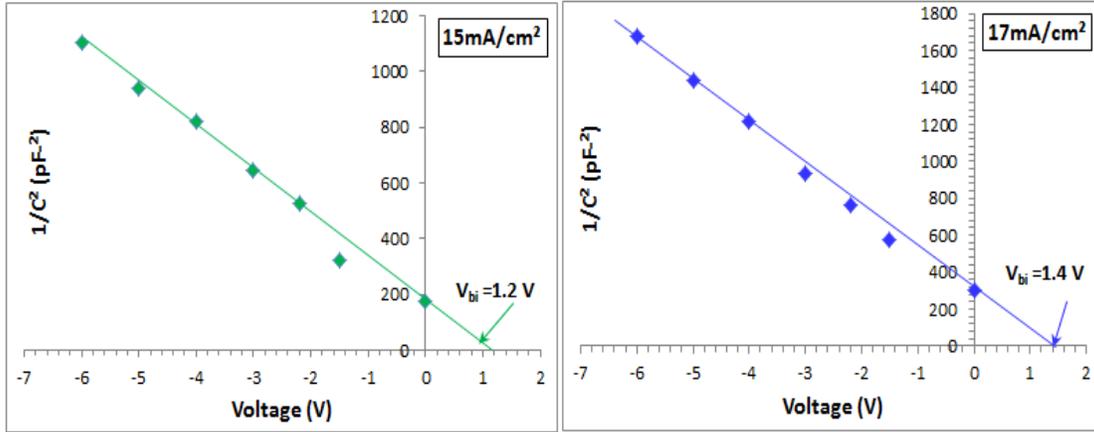


Figure A3(a). $1/C^2$ versus bias voltage of the Al/PSi/p-Si/Al

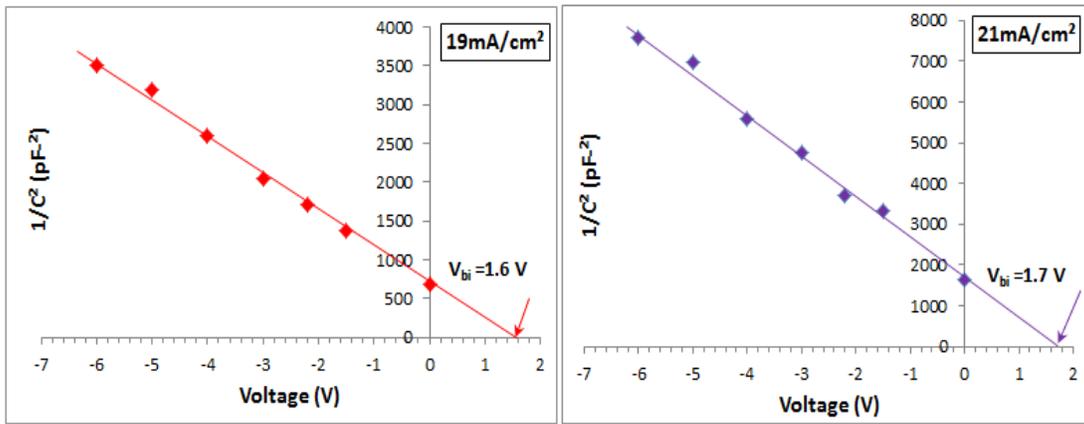


Figure A3(b). $1/C^2$ versus bias voltage of the Al/PSi/p-Si/Al